ParaPhrase: Parallel Patterns for Adaptive Heterogeneous Multicore Systems

Horacio Gonzalez-Velez, Kevin Hammond

1 National College of Ireland;
2 School of Computer Science, University of St. Andrews, Scotland.

Abstract

The ParaPhrase project aims to produce a new structured design and implementation process for heterogeneous parallel architectures, where developers exploit a variety of parallel patterns to develop component-based applications that can be mapped to the available hardware resources, and which may then be dynamically re-mapped to meet application needs and hardware availability.

We are exploiting new developments in the implementation of parallel patterns that will allow us to express a variety of parallel algorithms as compositions of lightweight software components forming a collection of virtual parallel tasks.

Components from multiple applications will be instantiated and dynamically allocated to the available hardware resources through a simple and efficient software virtualisation layer. In this way, we will promote adaptivity, not only at an application level, but also at a system level.

Finally, we are developing virtualisation abstractions across the hardware boundaries, allowing components to be dynamically re-mapped to either CPU/GPU resources on the basis of suitability and availability in a simple and straightforward way.
ParaPhrase:
Parallel Patterns for Adaptive Heterogeneous Multicore Systems
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W: paraphrase-ict.eu Twitter: paraphrase_fp7

Vision
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We are exploiting new developments in the implementation of parallel patterns that will allow us to express a variety of parallel algorithms as compositions of lightweight software components forming a collection of virtual parallel tasks.
Components from multiple applications will be instantiated and dynamically allocated to the available hardware resources through a simple and efficient software virtualisation layer. In this way, we will promote adaptivity, not only at an application level, but also at a system level.
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Objectives
• To develop high-level parallel design patterns that easily expose parallelism for a wide variety of parallel applications
• To develop efficient parallel implementations corresponding to these patterns that can be easily re-targeted to different hardware architectures.
• To define a virtualisation of the parallel software in the form of a low-level component model defining well-defined component state, life-cycle, and interfaces (use and provide) that allows the re-mapping to, possibly heterogeneous, hardware devices.
• To develop refactoring tools that support the parallel design process by allowing the straightforward inclusion of alternative parallelisations for the same software design.
• To develop adaptation mechanisms that dynamically and efficiently re-map software components to the available hardware components.
• To validate the overall ParaPhrase approach using a representative set of industrially-derived high-performance applications.
• To create a new user community with the help of which the new insights, techniques and experimental tools developed in the project.

Status
We have finished our first year and we have been positively evaluated.
The following items are currently progressing:
• ‘RISC’ Skeleton Set Ready
• Initial Refactoring tools available
• Static CPU/GPU Virtualisation underway
• User Application Set defined

Consortium
1. University of St Andrews (UK)
2. Robert Gordon University (UK)
3. Mellanox Technologies Ltd. (Israel)
4. Software Competence Center Hagenberg (Austria)
5. Erlang Solutions Ltd (UK)
6. University of Pisa (Italy)
7. High Performance Computing Center Stuttgart HLRS (Germany)
8. University of Torino (Italy)
9. Queen’s University Belfast (UK)
10. National College of Ireland (Ireland)

Coordinator:
Prof. Kevin Hammond
University of St Andrews (UK)
T: +44-1334 463241 F: +44-1334-463278
W: www.cs.st-andrews.ac.uk/~kh

References