Gecos: a source to source parallelization compiler for the automatic synthesis of parallel hardware accelerators

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Abstract:

Many embedded applications exhibit a large amount of coarse and/or fine grain parallelism that makes them well suited to hardware acceleration. However designing custom hardware accelerators that can take advantage of this parallelism remains a challenging task. This challenge has favoured the emergence of C to hardware compilers which enable the synthesis of a custom hardware accelerator directly from an algorithmic specification in C/C++. Even though such tools dramatically slash down design time, their ability to generate efficient accelerators is still limited, and relies on the designer to expose parallelism and use appropriate data layout in its source program. To help tackle this problem, we propose a source to source parallelizing compiler specifically targeted toward hardware synthesis tools. Such compilers are well known in the parallel computing world, and several frameworks exist (CETUS, ROSE). The transformations proposed by such tools are however targeted at standard parallel computing platforms (OpenMP, MPI) and are not well suited for C to hardware synthesis tools.

Among several transformations, our toolbox provides a loop and memory layout transformation framework based on the polyhedral model which provides a unified framework to express complex loop nests (and memory layout) transformations. This transformation engine uses a customized code-generation back-end with optimizations specifically targeted to custom parallel application specific accelerators (strength reductions, bit-accurate wordlength analysis, aggressive loop linearization, etc.).
Gecos: a source to source optimizing compiler for the automatic synthesis of parallel hardware accelerators

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GeCos is a C compiler infrastructure written in Java and leveraging on Model Driven Engineering software design principles and integrated within Eclipse IDE.

GeCos can be used as a Source to Source compiler for Custom Hardware Accelerator Synthesis. It supports bit-accurate C++ datatypes (Mentor Graphics Algorithmic C).

GeCos provides a powerful loop parallelization framework relying on the Polyhedral Model.

The Polyhedral Model Framework
- Powerful mathematical framework for loops
- Enables iteration wise dependence analysis
- Exposes parallelism and optimize memory size

Loop coalescing
- Reduces software pipeline overhead enabling effective multi dimensional pipeline.
- May not always be legal w.r.t. program data dependencies (we define legality condns)

SIMD control optimization
- Reduces the hardware control overhead in vectorized loops using "pipelined control"

Strength reduction and Bitwidth analysis
- Transformed kernels require complex control code (guards, loop bounds, array indices)
- Some operations (*,/) may have high area cost in hardware.
- We use strength reduction and polyhedral domain analysis to reduce hardware cost

High Level Synthesis back-end optimizations